Remarks:

Reconsideration of the application is requested.

Claims 1-6 and 10-15 remain in the application. Claims 11-12 and 15 have been amended. Claims 7-9 have been cancelled. Claims 1-6 have been withdrawn from consideration.

In item 3 on page 2 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.83(a) for not showing the feature(s) recited in claim 10. Shortly after mailing of the Office action, new drawings were entered into the instant application.

It is accordingly believed that the drawings meet the relevant requirements. Should the Examiner find any further objectionable items, Counsel would appreciate a telephone call during which the matter may be resolved. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In item 5 on page 3 of the Office action, claims 7-9 and 12-15 have been rejected as being anticipated by *Hsu* (US 5,468,657) under 35 U.S.C. § 102.

In item 6 on page 4 of the Office action, claim 10 has been rejected as being obvious over *Hsu* in view of *Sato et al.* (US 6,121,117) under 35 U.S.C. § 103.

The rejections have been noted, claims 7-9 have been cancelled and claim 10 has been re-written in independent form.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 10 as amended calls for, inter alia:

providing ***two*** silicon semiconductor substrates;

oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates;

selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X ***before*** the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X ***after*** the oxidation step into one of the silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and

partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer;

Hsu discloses a method for improving the electrical isolation between surface regions and underlying support regions in SIMOX buried oxide wafers by implanting nitrogen ions to approximately the same depth as oxygen ions are implanted during SIMOX processing.

The inventive concept of the invention of the instant application is to perform a diffusion process with neutral atoms of a passivating substance for bringing the passivating substance into the two semiconductor substances. A person skilled in the art knows the *Bonded Etched-back Silicon on Insulator* (BESOI) technique but he would not combine the BESOI technique with *Hsu* as *Hsu* merely teaches how to implant nitrogen ions into a buried oxide layer. Therefore, the invention as recited in claim 10 of the instant application is believed not to be obvious over *Hsu* in view of *Sato et al.*.

Another inventive concept of the invention of the instant application is to modify the BESOI method and to select the introducing step from the group consisting of introducing the passivating substance X into at least one of the ***oxide*** layers, introducing the passivating substance X ***before*** the oxidation step into one of the silicon semiconductor substrates, and

introducing the passivating substance X ***after*** the oxidation step into one of the silicon semiconductor substrates. In this case, the introduction of the passivating substance X can be performed simply by thermal doping (diffusion of the passivating substance from a passivating substance gas into the corresponding layer), since the layers to be passivated are uncovered before the joining of the two silicon semiconductor substrates. (see page 9 of the instant application for a detailed discussion)

It is accordingly believed to be clear that *Hsu* in view of Sato et al. do not suggest the features of claim 10. Claim 10 is, therefore, believed to be patentable over the art and since claims 11-15 are ultimately dependent on claim 10, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 10-15 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $ 110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

MARKUS NOLFF
REG. NO. 37,006

For Applicants

MN:cgm

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Version with markings to show changes made:

Claim 10 (amended). [The method according to claim 7, wherein the passivating substance X is introduced into the semiconductor structure] A method of fabricating a semiconductor configuration, which comprises the following steps:

providing a semiconductor structure having a base layer, an insulation layer, and a monocrystalline silicon layer;

introducing a passivating substance X between the insulation layer and the monocrystalline silicon layer during a fabrication thereof, by means of the following steps:

providing two silicon semiconductor substrates;

oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates;

selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating

substance X after the oxidation step into one of the silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and

partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer;

and

heat-treating the semiconductor structure with the passivating substance X, thereby causing the passivating substance to diffuse into an interface between the insulation layer and the monocrystalline silicon layer.

Claim 11 (amended). The method according to claim [7] 10, wherein comprises forming a covering oxide layer on the monocrystalline silicon layer.

Claim 12 (twice amended). The method according to claim [7] 10, which comprises patterning the monocrystalline silicon layer by etching away regions thereof down to an underlying insulation layer.

Claim 15 (amended). The method according to claim [7] 10, which comprises:

doping the monocrystalline silicon layer differently region by region by means of ion implantation; and

performing the doping step after the step of introducing the passivating substance X and the heat-treating step.